

**REMARKS**

Claims 1-8 are pending in the application. Of the claims, Claims 1 and 8 are independent claims. Claims 9-12 are newly added.

**Regarding objection to the drawings**

The drawings have been objected to under 37 CFR 1.83(a) for not showing every feature of the invention specified in claim 7. In response, claim 7 has been amended to clarify the Applicants' claimed invention. As shown in Fig. 1, and described in the Applicants' specification (*see* Page 5, line 23 to Page 6, line 7), the optical signal received by burst mode receiver in the central terminal is transmitted from remote terminals (RT) 120 over the PON 140. The objection is believed to be overcome and acceptance of the amendment to claim 7 is respectfully requested.

**Regarding rejection of under 35 U.S.C. 112, second paragraph**

Claim 5 has been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

In response, claim 5 has been amended to be dependent on claim 4 and to recite "the range of power levels is -32dBm to -7dBm" to clarify that power levels of the received packets range from -32dBm to -7dBm.

Removal of the rejection under 35 U.S.C. 112 and acceptance of Claim 5 is respectfully requested.

**Regarding rejection of claims under 35 U.S.C. 102(e)**

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,232,842 to Asano.

The Applicants' claimed invention is directed to an AC-coupled burst mode receiver. The burst mode receiver includes a converter that converts a received optical signal including a plurality of packets transmitted in burst mode into an electrical signal. A pre-amplifier coupled

through a capacitor to the converter receives an AC-coupled electrical signal from the converter and provides a corresponding voltage signal. The voltage signal has a driven edge time constant for each driven edge of the electrical signal and an undriven edge time constant that is extended and longer than the driven edge time constant for each undriven edge of the electrical signal. A differential amplifier having a hysteresis circuit is coupled to the pre-amplifier. The differential amplifier receives the voltage signal from the pre-amplifier and provides a digital signal corresponding to the voltage signal. The hysteresis circuit holds the digital signal in a particular state for each undriven edge of the voltage signal and changes the state of the digital signal for each driven edge of the voltage signal.

Asano is directed to a DC coupled burst optical receiver that includes a peak detector circuit that is used to determine the comparator decision threshold.

Asano does not teach or suggest the Applicants' claimed "pre-amplifier coupled to the converter through a capacitor, which receives an AC-coupled electrical signal". In contrast, Asano's optical receiver handling a burst signal is required to employ a DC coupling system and the output of the converter (pre-amplifier that converts an optical signal to a current signal) is coupled directly to the input of an amplifying circuit. (*See* Asano, Col. 1, lines 9-20; Fig. 8, 71 and 72.)

Furthermore, Asano does not teach or suggest the Applicant's claimed pre-amplifier which "outputs a corresponding voltage signal, the voltage signal having a driven edge time constant for each driven edge of the AC-coupled electrical signal and an undriven edge time constant that is extended and longer than the driven edge constant for each undriven edge of the AC-coupled electrical signal." Fig. 5C of Applicants' Specification illustrates this feature. As shown, the driven edge 130 is an edge amplified by the pre-amplifier that is caused by a data transition at the input. A driven edge moves away from the DC bias level of the pre-amplifier and is faster than an undriven edge. The undriven edge 132 is an edge amplified by the pre-amplifier that is not caused by a data transition at the input. Undriven edges decay toward the DC bias level of the pre-amplifier and are slower than driven edges. (*See* Applicants' specification Page 9, lines 17-28). In contrast, Asano discloses at most only driven edges, with no decay shown.

As recited in Claim 1, the pre-amplifier provides a driven edge time constant for each driven edge of a received signal and an undriven edge time constant for the decay of an undriven edge that is extended and longer than the driven edge time constant. With the capacitor coupled between the pre-amplifier and the converter, an undriven edge on the voltage signal is provided. (See Applicants' specification Page 12, line 16 – Page 13, line 8.) In contrast, Asano only shows driven edges with slow rise and fall times. (See Fig. 12a and Fig. 12b.)

Furthermore, Asano does not teach or suggest the Applicants' claimed "differential amplifier having a hysteresis circuit". Asano merely shows a comparator coupled to the output of amplifying circuit. (See Asano, Col 27, lines 38-41; Fig. 11, amplifying circuit 70, comparator 97.)

Accordingly, the present invention as now claimed is not believed to be anticipated by or made obvious from the cited art. Removal of the rejection under 35 U.S.C. 102(e) and acceptance of amended Claim 1 is respectfully requested.

Regarding rejection of claims under 35 U.S.C. 103(a)

Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,892,609 to Saruwatari in view of U.S Patent No. 6, 232,842 to Asano. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saruwatari in view of Asano as applied to claim 1 above, and further in view of U.S. Patent No. 5, 430, 765 to Nagahori. Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saruwatari in view of Asano and Nagahori as applied to claim 3, above and further in view of U.S. Patent No. 5,430,766 to Ota et al. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saruwatari in view of Asano as discussed in claim 1 above, and further in view of U.S. Patent No. 5,430,766 to Ota ("Ota-'766 ") or U.S. Patent No. 5,025,456 to Ota et al. (" Ota – '456")

Cited references Saruwatari, Nagahori, Ota-'766, Ota-'456, and Asano are each directed to a DC-coupled digital receiver including a peak detection circuit. Any discussion of AC-coupled burst mode digital receivers in the cited references is limited to the difficulty of implementing an AC-coupled receiver for burst mode data transmission. (See Ota-'456 Col. 1, lines 10-22; and Ota-'766, Col. 1, lines 25-35.) Indeed, Ota-'766 teaches away from AC-coupled burst mode receivers. (See Ota-'766, Col. 1, lines 30-35) The Applicants' claimed

invention is directed to an AC-coupled burst mode receiver which does not require a peak detector. Indeed Ota-'766 teaches away from AC-coupled burst mode receivers. (*See* Ota-'766, col. 1, lines 30-35.)

As already discussed, Asano does not teach or suggest a voltage signal with an undriven edge. Cited reference Saruwatari merely shows a data signal (which is comprised of purely driven edges) with the output of the peak detector circuit superimposed over the data. Cited reference Nagahori merely describes the operation of a peak detector in a digital data receiver. (*See* Fig. 1, peak detector 2; Fig. 2; and Fig. 4(B).)

Regarding the rejection of independent claim 8, Ota-'766 does not suggest the use of AC coupling for a burst mode receiver. As already discussed, Ota-'766 teaches away from the use of AC coupling for a burst mode data receiver. (*See* Ota -'766, col. 1, lines 30-35.)

Even if combined, the cited references do not teach or suggest the Applicants' claimed pre-amplifier which "outputs a corresponding voltage signal, the voltage signal having a driven edge time constant for each driven edge of the AC-coupled electrical signal and an undriven edge time constant that is extended and longer than the driven edge constant for each undriven edge of the AC-coupled electrical signal."

Accordingly, the present invention as now claimed is not believed to be made obvious from the cited art. In view of the foregoing, removal of the rejections under 35 U.S.C. 103(a) and acceptance of Claims 1-12 is respectfully requested.

#### Information Disclosure Statement

An Supplemental Information Disclosure Statement (SIDS) is being filed concurrently herewith. Entry of the SIDS is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,  
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